CLAIMS

What is claimed is:

1. A method of assessing timing of PCI signals, comprising:

initiating a test mode within a host adapter board;

generating a clock signal for the host adapter board;

generating PCI signals within the host adapter board;

electronically selecting one or more PCI signal lines of the host adapter board; and

assessing timing of the one or more PCI signals from the PCI signal lines.

2. The method of claim 1, the step of electronically selecting comprising utilizing addresses within memory of the host adapter board to select the one or more PCI signal lines.

3. The method of claim 2, further comprising storing addresses within the memory.

4. The method of claim 3, the step of storing comprising loading addresses into I/O controller memory.

5. The method of claim 1, the steps of generating PCI signals and electronically selecting comprising utilizing an I/O controller of the host adapter board.

6. The method of claim 1, the step of initiating a test mode comprising utilizing a jumper connected between the host adapter board and an external electronic device.

7. The method of claim 1, the step of electronically selecting comprising cycling through addresses within memory of the host adapter board.

8. The method of claim 1, the step of assessing comprising utilizing a logic analyzer.

9. The method of claim 1, the step of generating a clock signal comprising utilizing a signal generator connected with the host adapter board.

10. The method of claim 1, the step of assessing comprising assessing one or both of slew rate and clock-to-signal valid of the PCI signals.

11. A system for assessing timing of PCI signals, comprising:

a host adapter board responsive to a test mode initialization to generate PCI signals within the host adapter board, the host adapter board having internal memory for storing addresses for PCI signal lines of the host adapter board, the host adapter board adapted to receive an external clock signal and being configured to select one or more of the PCI signal lines, based on the addresses, for output from host adapter board; and

a PCI test controller for assessing PCI signals from the output and relative to the clock signal.

12. The system of claim 11, the PCI controller assessing one or both of clock-to-signal valid and slew rate from the output.

13. The system of claim 11, the host adapter board further comprising an I/O controller that includes the internal memory, the I/O controller operable to facilitate communications between the host adapter board and an electronc device connected with the host adapter board.

14. The system of claim 13, the controller having a switch for toggling the one or more PCI signal lines based upon the addresses.

15. The system of claim 14, the switch and memory cooperating to cycle through the addresses such that different PCI signals connect with the output, over time.

16. The system of claim 11, further comprising a generator for generating the PCI signals.

17. A system for assessing timing of PCI signals, comprising:

means for initiating a test mode within a host adapter board;

means for generating a clock signal for the host adapter board;

means for generating PCI signals within the host adapter board;

means for electronically selecting one or more PCI signal lines of the host adapter board; and

means for assessing timing of the one or more PCI signals from the PCI signal lines.

18. The system of claim 17, the means for generating PCI signals and means for electronically selecting comprising an I/O controller of the host adapter board, the I/O controller further comprising internal memory for storing addresses of the one or more PCI signal lines.

19. The system of claim 18, further comprising means for cycling through the addresses such that, over time, the means for assessing assesses different PCI signals of the host adapter board.

20. The system of claim 17, the means for assessing comprising means for determining one or both of clock-to-signal valid and slew rate for the one or more PCI signal lines.